GUC Advanced Solution for HPC Era

GUC

ABSTRACT

With emerging application (such as cloud & AI), High Performance Computing feature is getting more and more important. Consider to design complexity and power consumption, leading-edge technology (N7) and advanced package (CoWos) are the key factors to boost this application. GUC has developed our design flow of N7 and package experiences of CoWos which we proved in test chip and also engaged in customer chip.

This presentation will share GUC's solution and experiences in N7 implementation and CoWos package, and also including some achievments to demonstrate the capabilities.

GUC
The Flexible ASIC Leader

GUC Advanced Solution for HPC Era

DSP/Gary Huang

Agenda

- Why HPC matters?
- What are the challenges?
- GUC's preparation
- Summary

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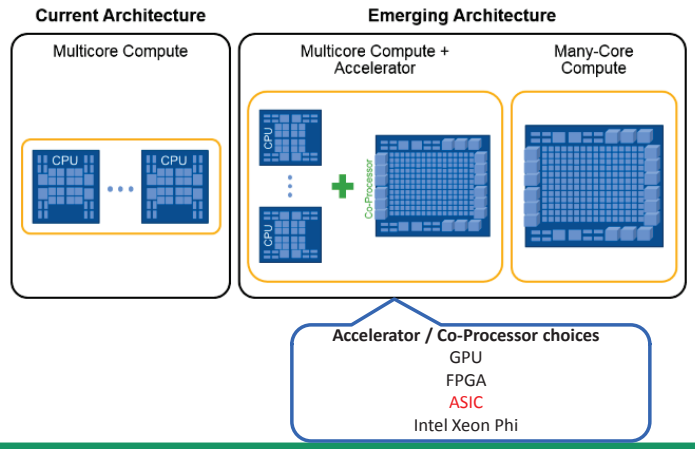
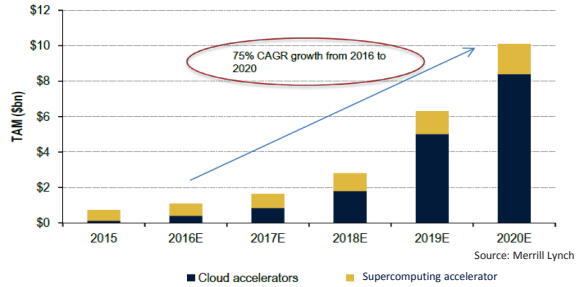
High Performance Computing Architectures

- Current and Emerging High-Performance Computing Architectures



DL Market Trend & Technology Insight

- **Deep learning processor chips will be the fastest growing application market in semiconductors by 2020**
- **Cloud data center will dominate by 2020**
  - 50% of servers in 2020 will be in cloud
  - At least 1/3 of the cloud servers will use accelerators in some form.



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Challenges for HPC Segment

- **Advanced technology node enablement**
  - N7, CoWoS with HBM2
- **Huge physical design (> 300mm^2)**
  - Data flow analysis and congestion prevention for large amount of inter-IP connectivity
  - Capacity / TAT enhancement for comprehensive verification jobs in billion-gate design
- **With repeated block / tile**
  - Requires design flow methodology capable of dealing with high peak power & dynamic power, whole chip IR drop.
  - DFT methodology

Challenges for HPC Segment (cont'd)

- **Power and timing closure challenges**
  - Power network co-design across package ball, bump, and die
  - High R mitigation in N7/N16 advanced technology nodes
- **Package**
  - Thermal simulation for high power
  - High speed signaling
  - Production testing technique for high power chip (200~400W)
  - CoWoS + HBM2 PHY/CTRL

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For Advanced Node (N7)

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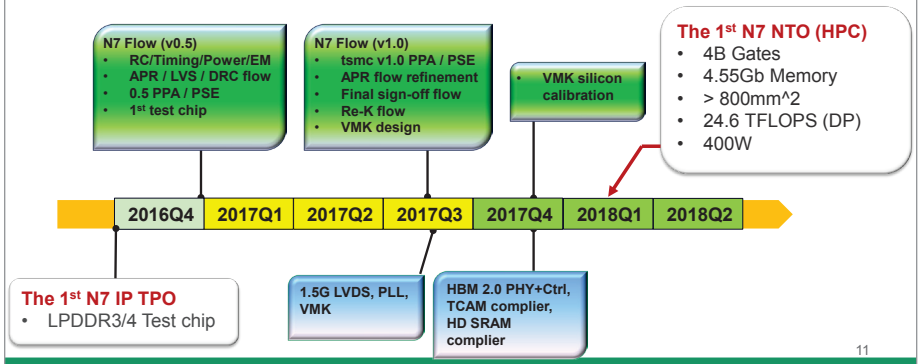
GUC N7 Milestone

- N7 V1.0 design flow is ready now
- The 1st N7 IP test chip was taped out in early Q4'16
- We will have another 2 IP test chip tapeouts in Q3'17 and Q4'17
- N7+ in 2018 (under plan)



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GUC N7 Engagement

Application	Biz Type	TPO	IP Requirements
OTN	TK1	2018	Serdes, PCIe
Switch	TK1	2018	Serdes, PCIe, TCAM, 2P SRAM,
Switch	TK2	2018	Serdes, 1P/2P SRAM, TCAM
Switch	TK2	2019	SerDes
HPC	TK1	2019	Serdes, PCIe, HBM
HPC	TK1	2018, 2019	Serdes (low power), 2P SRAM, PLL, VMK
HPC	TK1	2018	Serdes, PCIe, TCAM
HPC	TK1	2018	SerDes
HPC	TK1	2018	PCIe
HPC	TK2	2018	PLL, VMK
HPC (CPU)	TK1	2018	DDR4, PCIE4, SRAM, PLL
Base Station	TK1	2018	Serdes, PCIe, LPDDR

The 1st customer's N7 tapeout in Q1'18 under HPC segment

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For IP Requirements

IP Portfolio for HPC Application (May'17)

Type	N16	N7
56G SerDes	Q4'18	Q4'18
28G SerDes	Q2'18	TBD
16G SerDes	Q2'18	TBD
PCIe 4 PHY	Q2'18	TBD
DDR3/4 LPDDR 3/4	A	Q2'18 (LP/DDR5)
HBM 2.0	08'17	Q2'18
TCAM	Q3'17 (Marco) Q1'18 (Complier)	Q3'18 (Complier)
HD 1P-RF specialty memory	Q1'18 (Complier)	Q1'18 (Macro) Q3'18 (Complier)

- **Standard support :**
  - PAM-4: CEI-56G-USR to CEI-56G-LR
  - NRZ: CEI-28G-USR to CEI-28G-LR
  - All IEEE-802.3 PHY layer causes
- **Ref clk: 156.25, 125, 25 MHz**
- **Power @ TT, per lane**
  - 56Gbps PAM-4: 300mW @LR
  - 28Gbps NRZ: 200mW @LR

- **100~110 mW/Lane**
- **16 GHz**
- **Support bifurcation**

- **PHY + CTRL**
- **Speed: 4267 Mbps (LP/DDR4); TBD (LP/DDR5)**

- **HBM2.0 IP Total Solution (CTRL + PHY + IO)**
- **2.4 Gbps / pin**

- **Target performance @ SSGNP with 0.9xVcc @ 125C: 1GHz for N16FFC, 1.5GHz for N7**

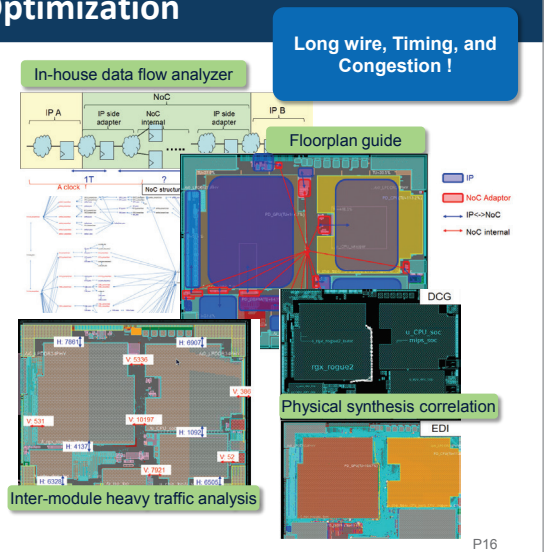
- **Performance > 600 MHz @ WCL**
- **10~30% area reduction over tsmc SP SRAM**

A: Available, TBD: To Be Determined, -: No Plan
MM/Q'YY: Silicon verified

For Physical Design

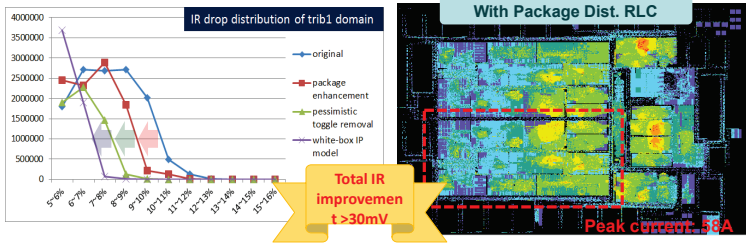
Data Flow Driven Optimization

- Data Path Structure & Critical Timing Analysis
- Floorplan Guide Insertion & Tuning
- Inter-Module Heavy Traffic Analysis
- Physical Synthesis (DCG vs. EDI) Correlation



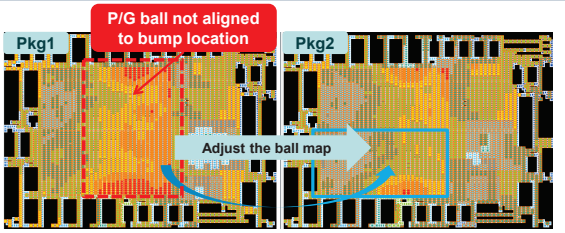
Power Integrity in Big Design

- **Accurate package distributed RLC extraction in IR sign-off**
- **Comprehensive solutions of voltage drop resolution**
  - Package layout and P/G ball enhancement, Decap insertion
  - Pessimism removal of instance toggle scenario
  - White-box IP model to share P/G bumps
- **Achieve dynamic IR drop within 10% for 240Mgate design**

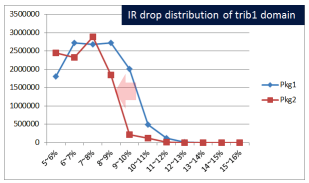


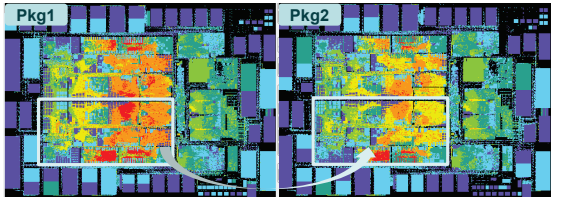
Power Integrity – Package Co-Design Influence

- **Package distributed RLC helps to identify co-design weak spot**
- **Package & P/G ball enhancement pushes IR reduction by ~10mV**



Reduce voltage drop at VDD bump pad

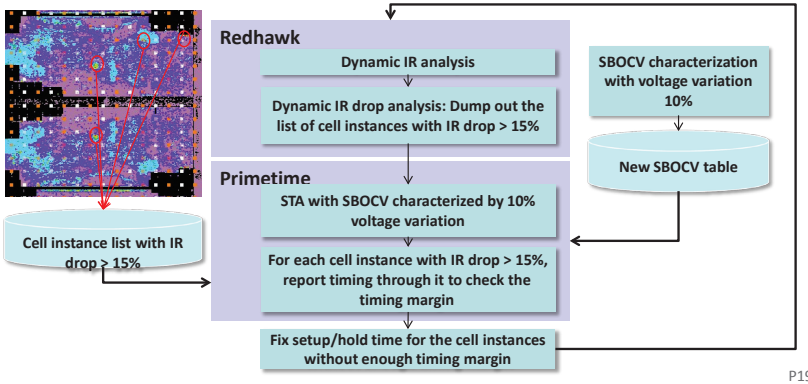




Reduce cell instance voltage drop

Voltage Variation Aware Timing Sign-off

- Fix dynamic IR hot spot to be under target 15%
- Collect cell instances with IR drop > 15%
- Perform STA with extra OCV on IR hot-spot cells with IR drop >15%



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For DFT

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DFT Service Focus for HPC

- **HPC application feature**
  - Huge design / System self-test / Faulty cores identification / Limited channel spacing / HBM

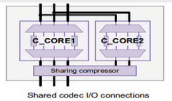
HPC Feature	DFT Solution / Strategy
Huge design Tile base design	DFT solutions for huge design
System self-test System self-test for Logic or Memory	System Logic / SRAM BIST solution
Faulty cores identification Identify fail cores and bypass	SCAN / SRAM BIST planning for fail cores identification
Limited channel spacing Light channel or channel less between blocks	DFT plan with routing resource consideration
High bandwidth memory (HBM) CoWoS with HBM	CoWoS interconnect test between SoC and HBM

DFT Solution for HPC

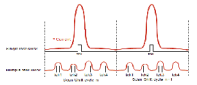
- **DFT solution for huge design**

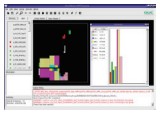
Target	Methodology
Big design scale	Hierarchical SCAN and MBIST planning, Smart Memory BIST grouping
Test pattern and pin count tradeoff	Scan compression, multi mode, sharing codec scan, Ultra compress
DFT mode power	Power-aware scan clock planning, Shift power control (SPC), Power aware ATPG
Yield	SRAM repair solution

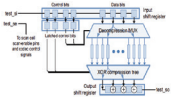
Hierarchical Scan Plan

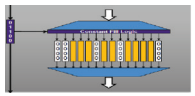


Sharing Codec Scan IO


Multi phase scan clock


Smart Memory BIST Grouping

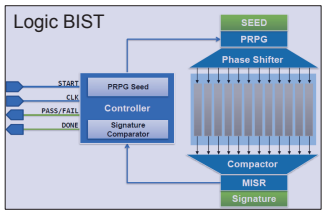

Ultra Compression

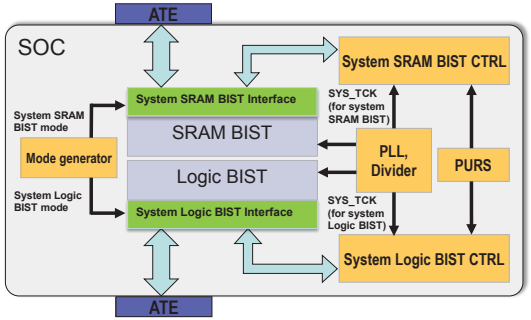

Shift Power Control

DFT Solution for HPC (Cont.)

- **Logic/SRAM BIST provide boot on self test and in system operation test**

System BIST operation scenario
Boot on self test
In system operation test

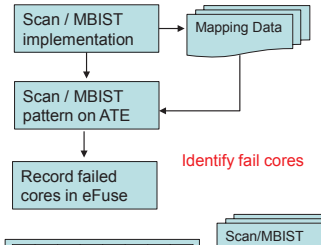


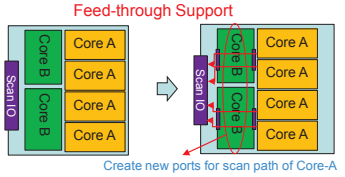


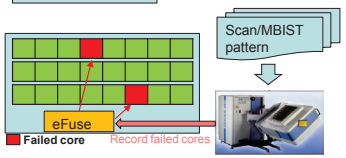
GUC : Act for Logic/SRAM BIST implementation
Customer : Act for re-use/integrate Logic/SRAM BIST for function safety consideration

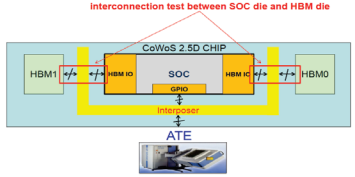
DFT Solution for HPC (Cont.)

- **SCAN / SRAM BIST planning for fail cores identification**
- **DFT plan with routing resource consideration**
- **CoWoS interconnect test between SoC and HBM**





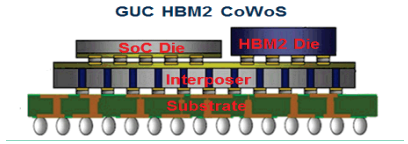




For CoWos

GUC's Unique Value

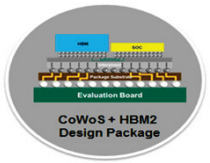
- **HBM2 + CoWoS**
  - **An integrated technology & design solution**
    - World class HBM2 Controller + PHY solution
    - In-house Interposer design, simulation, and DFT
  - **Proven by TSMC flow.**
  - **Proven with WW tier-1 memory die manufacturers.**



TSMC-GUC HBM2 & CoWoS Project

- **Silicon-validated CoWoS & JEDEC-compliant HBM2 system design package solution**

System design
- 2.0Gbps HBM2 PHY
- 2.0 Gbps CoWoS interconnect
- 2.0Gbps HBM2



HBM memory

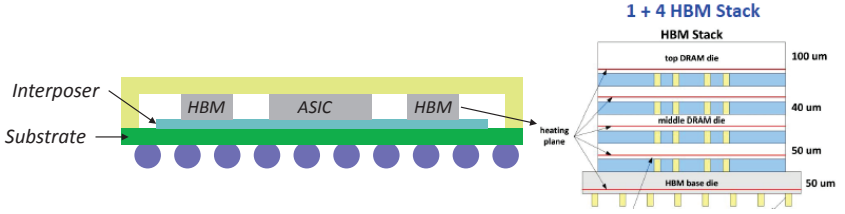
HBM2
- Models (DFT, simulation, HSPICE, AC/DC timing)
- Physical ball out (GDS)

CoWoS HBM2 integration guide
- Physical verification (SI/PI/LVS/DRC/IR-drop)
- Interposer & combo bump GDS

HBM PHY & Controller
- Models (RTL, timing, simulation, verification, LEF)
- EVB

CoWoS Thermal Co-simulation Capability

- **Junction temperature requirement is critical to high power and complicated CoWoS package design**
- **We build the consolidated model based on real geometry, material property and perform 2.5D stack-up of ASIC die and 4 HBM analysis**
  - Package and interposer modeling
  - Package thermal analysis
  - System thermal analysis considers air flow, heat sink and active fan selection



Cabinet size follow JESD 51-2 (304.8x304.8x304.8mm³)

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Summary

- HCP segment will be in high growth in coming years and ASIC/coprocessor is in strong demand.
- There are several challenges in HPC segment, such as huge/complex design, power integrity, DFT etc.
- Good experiences in advance node in design flow and also developed related IP for customer engagement.
- Comprehensive physical design and DFT methodology
- Work with tier-1 partner in offering HBM/CoWos solution to shorten customer's time to market.

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Thank you !

Uncompromising Performance

www.guc-asic.com

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